Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte HAJIME ARAI

Appeal No. 1998-2966
Application 08/605,566[1]

ON BRIEF

Before JERRY SMITH, BARRETT, and FLEMING, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-4.

BACKGROUND

The disclosed invention addresses a problem which occurs in prior art non-volatile semiconductor memory devices as shown in figures 7 and 8. An impurity ion 16 invading from a defective portion of passivation film 12 moves in interconnection layer 11 or an interface between interconnection layer 11 and interlayer insulating film 9 and might penetrate underlying insulating film 8 and side wall 17 to reach floating gate electrode 5 (specification, p. 5, lines 20-25). These impurity ions may cancel the electric charge of the electrons stored in the floating gate electrode 5 and, in an extreme case, data stored in the non-volatile memory cell is inverted, leading to defectiveness of the cell (specification, p. 2, lines 16-25). The disclosed invention provides an impurity introduction conductive layer between the interconnection layer 11 and the interlayer insulating film 9, which traps the invading impurity ion as illustrated in figure 1.

Claim 1, the sole independent claim, is reproduced below.

> 1. A non-volatile semiconductor memory device, comprising:

a control electrode formed on said electric charge storage electrode with an interelectrode insulating film interposed therebetween;

an underlying insulating film with no impurity introduced formed so as to cover a surface of said semiconductor region, said electric charge storage electrode, and said control electrode;

an interlayer insulating layer having a contact hole exposing a surface of one of said pair of impurity regions and formed so as to cover said underlying insulating film;

an impurity introduction conductive layer of the second conductivity type formed in said contact hole so as to cover said underlying insulating film exposed to an inner surface of said contact hole; and

an interconnection layer electrically connected to said impurity regions in said contact hole.

The Examiner relies on the admitted prior art (APA) at figures 7 and 8 and the related discussion, and on the following prior art:

Higuchi	5,466,971	November 14, 1995 (filed October 31, 1994)
Kobayashi	5,500,816	March 19, 1996 (filed February 28, 1994)

Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi or the APA in view of Higuchi.

We refer to the final rejection (Paper No. 10) and the

brief (Paper No. 18) (pages referred to as "RBr__") for Appellant's arguments thereagainst.

OPINION

The claims stand or fall together with claim 1 (Br4).

The APA and Kobayashi disclose the claimed non-volatile semiconductor memory device except for the claimed "impurity introduction conductive layer of the second conductivity type formed in said contact hole so as to cover said underlying insulating film exposed to an inner surface of said contact hole." The devices in the APA and Kobayashi suffer from the problem addressed and solved by the claimed invention, i.e., impurity ion invasion of a floating gate electrode.

Higuchi discloses that in conventional semiconductor devices, after contact holes are formed in an insulating layer lying over a conductive layer in the form of an impurity diffusion layer formed in the semiconductor substrate, a metal coating is provided thereover, and the conductive layer having the semiconductor nature and the wiring metal are in direct contact with each other (col. 1, lines 44-50). A problem with downsizing the diameter of the contact hole as part of downsizing

contact portion between the semiconductor and metal due to the difference in energy level" (col. 1, lines 53-58). Higuchi overcomes this problem by providing a multilayer interconnection layer including a conductive silicon layer 6 containing impurities such as phosphorus, arsenic, or boron (col. 6, lines 46-50), a barrier metal layer 7 contacting the conductive silicon layer 6, and a metal wiring layer 8 contacting the barrier metal layer 7 (col. 6, lines 37-67). The use of a conductive silicon layer between the conductive region having the semiconductor property and the metal wiring layer is said to minimize the resistance and Shottky barrier (col. 7, lines 16-29). The multilayer interconnection layer 6/7/8 is disclosed in several different embodiments (e.g., figures 1, 4, 7. 9, and 13); however, none of the embodiments are to a non-volatile semiconductor memory device having a floating gate electrode that might have the problem of impurity ion invasion.

In the final rejection, the Examiner concluded (FR4-5):

> Higuchi ('971) teaches the concept [of including an impurity introduction conductive layer in the contact hole], such that it would have been obvious to one having ordinary skill in the art at the time of the invention to include [sic, provide] the memory device of the admitted prior art

> Higuchi] would inherently [have] prevented an [sic] p-type impurity [from being] introduced into the underlying insulating film. Therefore, this limitation is also met by the applied prior art device. [Emphasis added.]

Appellant argues that this is the epitome of improperly relying on Appellant's disclosure for the requisite motivation (Br5). It is argued that the Examiner committed clear legal error in relying on the doctrine of inherency and in concluding that one of ordinary skill in the art would have recognized that the claimed invention would inherently flow if the references are combined. Appellant argues "that the Examiner's back door approach of concluding that if the applied prior art is combined then the claimed invention would inherently result, has been repeatedly judicially condemned as confusing obviousness with inherency" (Br11). In summary, it is argued that the Examiner has not established the requisite motivation to support a prima facie case of obviousness and has erroneously relied upon the doctrine of inherency (Br11-12).

We agree with Appellant that the Examiner's reasoning expressed in the final rejection is erroneous. There is no reason in the references why one of ordinary skill in the art, if

that it would have been obvious to incorporate the conductive layer of Higuchi into the APA or Kobayashi "in order to provide more protection for the gate electrodes, so that the performance of the memory cells can be improved" (FR4) clearly and impermissibly relies on Appellant's disclosure for the motivation. While it is uncontested that the provision of a conductive silicon layer as taught by Higuchi in the APA or Kobayashi would inherently perform the (unclaimed) function of preventing floating gate ion invasion, "a retrospective view of inherency is not a substitute for some teaching or suggestion which supports the selection and use of the various elements in the particular claimed combination," In re Newell, 891 F.2d 899, 901, 13 USPQ2d 1248, 1250 (Fed. Cir. 1989). Thus, the Examiner's reasoning in the final rejection is not persuasive.

In the examiner's answer, the Examiner modifies the obviousness reasoning to conclude (EA5; see also EA7, EA9):

> [I]t would have been obvious to one of ordinary skill in the art at the time the invention was made to include [sic, provide] the memory device of the admitted prior art or Kobayashi with the impurity introduction conductive layer formed in the contact hole . . . because it would have imparted to the memory device of the admitted prior art or Kobayashi the advantageous benefits of minimizing the

Claim 1 is drawn to a non-volatile semiconductor memory device structure. The function of the impurity introduction conductive layer of preventing floating gate ion invasion is not recited. While the function does not have to be recited, it is improper to narrow the scope of the claim by implicitly reading in disclosed limitations from the specification which have no express basis in the claims. See In re Prater, 415 F.2d 1393, 1404, 162 USPQ 541, 550 (CCPA 1969); In re Priest, 582 F.2d 33, 37, 199 USPQ 11, 15 (CCPA 1978) (inferential limitations are not to be read into the claims); In re Self, 671 F.2d 1344, 1348, 213 USPQ 1, 5 (CCPA 1982) ("Many of appellant's arguments fail from the outset because . . . they are not based on limitations appearing in the claims."). Thus, it is not necessary that the combination of references teach or suggest solving the floating gate ion inversion problem because it is not claimed.

We agree with the Examiner that Higuchi suggests providing an impurity introduction conductive layer of a second conductivity type in the contact hole of the APA or Kobayashi to minimize the resistance and Shottky barrier. This teaching applies regardless of the type of semiconductor device. Although

obviousness. See In re Dillon, 919 F.2d 688, 693, 16 USPQ2d 1897, 1901-02 (Fed. Cir. 1990) (en banc) (holding that an invention may be obvious for reasons the inventor did not contemplate) (overruling-in-part In re Wright, 848 F.2d 1216, 6 USPQ2d 1959 (Fed. Cir. 1988)). It is sufficient that the collective teachings of the references suggest the claimed structure. Appellant does not address, and therefore has not shown error, in this reasoning. We sustain the rejection of claims 1-4 for the reasons stated in the examiner's answer.

We comment on one other issue. The Examiner asserts for the first time during prosecution, in the examiner's answer, that there is no evidence that the claimed invention solves the floating gate ion invasion problem of a non-volatile semiconductor device and that it is not clear how the positively charged ions are trapped (EA8-9). Appellant argues that the Examiner has made inaccurate factual assumptions (RBr1-2) and that the Examiner has not provided a sound technological basis for challenging the assertions in the specification (RBr4). We agree with Appellant that the Examiner appears to be merely speculating and provides no persuasive evidence or reasoning to

CONCLUSION

The rejection of claims 1-4 is sustained.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

JERRY SMITH Administrative Patent Judge	)
LEE E. BARRETT Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
MICHAEL R. FLEMING Administrative Patent Judge	)

Appeal No. 1998-2966
Application 08/605,566

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005